ULTRA-THIN Si CHANNEL CMOS WITH IMPROVED SERIES RESISTANCE

ABSTRACT OF THE DISCLOSURE

Thin silicon channel SOI devices provide the advantage of sharper sub-threshold slope, high mobility, and better short-channel effect control but exhibit a typical disadvantage of increased series resistance. This high series resistance is avoided by using a raised source-drain (RSD), and expanding the source drain on the pFET transistor in the CMOS pair using selective epitaxial Si growth which is decoupled between nFETs and pFETs. By doing so, the series resistance is improved, the extensions are implanted after RSD formation and thus not exposed to the high thermal budget of the RSD process while the pFET and nFET can achieve independent effective offsets.